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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,087	08/21/2006	Wolfgang Fey	AP 10889	4162

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EXAMINER	
AHMED, ENAM	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/590,087	FEY ET AL.	
	Examiner	Art Unit	
	ENAM AHMED	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *25-47* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *25-47* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non - Final

This office action is in reply to applicant's RCE filed on 12/22/10.

Claim Objection

1. Claim 25 is objected to because of the following informalities: claim 25 has the word "from" listed twice. Appropriate correction is required.

Response to applicant's arguments

1. Applicant's arguments with respect to claim 25 has been fully considered, however are not found persuasive.

Response to applicant's remarks

With respect to claim 25, the applicant argues the Shipton et al. reference does not teach an error checking circuit with multiple independent processor cores.

The Examiner respectfully disagrees with the statement, and points out in para. [1664], where it is taught that, the configuration registers are programmed by the CPU and two identical LSS master units that generate the signaling protocols on the two LSS buses as well as interrupts to the CPU, thus the two LSS master units, are serving as

the processor cores. Further, in para [1666], it also mentions that the configuration registers in the LSS block are programmed via the CPU interface. Thus, the Shipton et al. reference teaches an error checking circuit with multiple independent processor cores ([1664] and [1666]).

35 U.S.C. 102

a. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 25-47 are rejected under 35 U.S.C. 102(e) as being unpatentable over Shipton et al. (Pub. No. 2006/0052962).

With respect to claim 25, the Shipton et al. reference teaches sending a pair of logically complementary error signals from respective first and second independent processor cores to at least one further component (2) ([1656], [1664 – the LSS master units are the processor cores], [1666], [1521], [1565] and see fig. 63A, CPU – error

signals such as cpu_rwn and cpu_acode are sent to configuration registers – signals such as Ccpu_time_sel, cpu_rwn and cpu_acode are the complimentary signals being sent from the CPU. These error signals are being sent together in parallel due to the fact that the CPU detects some inconsistency with the information being provided, and needs more accurate data, so in order to determine the more accurate data, it sends signals which are alike or complimentary in some way to the configuration registers to derive the accurate data); and evaluating the error signals in the at least one further component when each of the error signals has maintained its respective logic state for at least a minimum pulse length (see fig. 63A, Timing Pulse Generator and [1581] – After the configuration registers receive the error signals such as cpu_adr, cpu_time_sel and cpu_rwn, they are processed within the configuration registers and then signals such as free_run_wen and timer_start_value are sent to the timing pulse generator in addition to also writing data as seen in the figure, wherein the timing pulse generator compares the signals with the built-in free running counter to determine time elapsed between events at system clock accuracy and re-sends signals such as free_run_cnt and pulse_timer_status to the configuration registers based on the error signals. Further, it is also mentioned that the free running counter can also be used as an input source in low-security random number generator).

With respect to claim 26, the Shipton et al. reference teaches wherein the further component is a mixed-signal module (see fig. 63A, Timing Pulse Generator).

With respect to claim 27, the Shipton et al. reference teaches wherein in the event of a sequence of pulses on at least one of the error signals with a distance between the pulses that is smaller than the minimum pulse length, the time of the sequence of pulses output over the a respective one of the error signals is extended with respect to the actual pulse sequence time ([3237]).

With respect to claim 28, the Shipton et al. reference teaches comprising filtering the error signals ([1524]).

With respect to claim 29, the Shipton et al. reference teaches wherein at least one watchdog time window (17) is predetermined in the integrated circuit or in the further component (2), within which at least one artificially produced error signal or error signal pattern is generated and tested so that the error detection circuits become self-testable (see fig. 63A, Watchdog timer - also see wdog_wen and wdog_time_cnt).

With respect to claim 30, the Shipton et al. reference teaches wherein the watchdog time window (17) has a delay time TWindowDelay, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time TWindowDelay (see fig. 63A, Watchdog timer – see wdog_time_thres).

With respect to claim 31, the Shipton et al. reference teaches wherein the delay time TWindowDelay is longer than a filter time TFilter of filter(s) (7, 7') processing the error signals ([1524]).

With respect to claim 32, the Shipton et al. reference teaches wherein the time window TWindowDelay is set in the further component (2) by way of an interface (5) connected to at least one microprocessor chip or multiple processor uc (see fig. 63A, Generic Timers).

With respect to claim 33, the Shipton et al. reference teaches wherein a condition TWindowDelay is satisfied in excess of the filter time TFilter ([1524]).

With respect to claim 34, the Shipton et al. reference teaches wherein the delay TWindowDelay approximately corresponds to twice the time TFilter ([1524]).

With respect to claim 35, the Shipton et al. reference teaches extending durations of pulses on the error signals ([3237]).

With respect to claim 36, the Shipton et al. reference teaches wherein a test of the error signals (3, 4) is performed with the aid of an interface (5) (see fig. 63A, Timing Pulse Generator).

With respect to claim 37, the Shipton et al. reference teaches wherein the error signals are filtered by filters (7, 7') with a defined filter time TFilter ([1524]).

With respect to claim 38, the Shipton et al. reference teaches wherein the pulse width TMin is set to a value of at least 30 nanoseconds approximately ([3237]).

With respect to claim 39, the Shipton et al. reference teaches at least one microprocessor chip or multiple processor microcontroller (1) or microprocessor module (see fig. 63A, CPU); at least one additional separate component (2) having separately arranged power elements (see fig. 63A, Configuration Registers); and one or more pulse extending devices or signal delaying devices for outputting error pulses (6, 6') one after another through at least one error line (3, 4) (see fig. 63A, Timing Pulse Generator). See detailed explanation in claim 25 above.

With respect to claim 40, the Shipton et al. reference teaches one or more filters (7, 7') for filtering the error pulses transferred through the error lines (3, 4) ([1524]).

With respect to claim 41, the Shipton et al. reference teaches at least one microprocessor chip or multiple processor microcontroller (1) (see fig. 63A, CPU); at least one additional component (2) having separately arranged power elements , wherein a complementary pair of error signals transferred between the at least one microprocessor chip or multiple processor .mu.C (1) and the at least one additional

component (2) (see fig. 63A, Configuration Registers – the registers receive the error signals from the CPU); and FILTERS for filtering error pulses (6, 6') through associated ones of the error signals (see fig. 63A, Timing Pulse Generator). See detailed explanantion in claim 25 above.

With respect to claim 42, the Shipton et al. reference teaches wherein each filter (7, 7') is configured as a digital forward/backward counter ([3237]).

With respect to claim 43, the Shipton et al. reference teaches wherein the chips or components are interconnected by at least one bus (5) and at least one error line (3, 4) (see fig. 63A, CPU).

With respect to claim 44, the Shipton et al. reference teaches wherein the circuit includes hardware test structures, with the aid of which a test of the at least one error line (3, 4) can be performed using an interface (5) (see fig. 63A).

With respect to claim 45, the Shipton et al. reference teaches wherein the microprocessor chip (1) or the additional component comprises at least one watchdog window circuit (50) (see fig. 63A, Watchdog timer).

With respect to claim 46, the Shipton et al. reference teaches wherein the watchdog window circuit (50) predefines a watchdog time window (17), and the

watchdog time window (17) has a delay time TWindowDelay, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time TWindowDelay (see fig. 63A, Watchdog timer – see wdog_time_thres).

With respect to claim 47, the Shipton et al. reference teaches wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal(s) of the at least one error line (3, 3') ([1524]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman, can be reached on 571-272-3644.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

9/25/11

/Scott T Baderman/

Supervisory Patent Examiner, Art Unit 2114